

IN THE DRAWINGS:

Kindly substitute the single sheet of formal drawings enclosed (in triplicate) for that originally filed in the case. A letter to the Official Draftsman is enclosed herewith. No new matter has been added.

R E M A R K S

Reconsideration of the above-identified patent application is respectfully requested in view of the following remarks. Claims 1, 2, 4 through 7, 11, 12, and 14 remain in the application.

The invention features a circuit board laminate structure having three-layers and comprising an inner power core layer 14 that is connected between two signal core layers 12 (our emphasis), as shown in the three separate embodiments depicted in exploded views of FIGURES 1, 2, and 3. Upon lamination of the signal layers 12 to the inner core layer 14, the circuit board structure is electrically connected. The laminated

circuit board inner power core layer 14 comprises filled via through holes 16 of conductive adhesive. The conductive power core layer vias make contact with the metal pads 3 of conductive vias 15, of the respective outer signal core layers 12 (our emphasis).

The rejection of the claims under 35 U.S.C. §102(b) as anticipated by DiStefano et al. is respectfully traversed for the following reasons:

The patent to DiStefano et al. teaches the construction of a multi-layered laminate comprising five layers shown in FIGURES 1 and 3. By contrast, Applicants only show three layers in embodiments 10, 20, and 30. Please observe that because there are only three layers in Applicants' structure, it is possible to have the center (second) layer as a power core layer. There is no such teaching of a power core layer in DiStefano et al. Neither are there any sandwich layers (first and third) layers in DiStefano's device described as signal core layers, as claimed in Claim 2. Applicants' vias are electrically connected at their pads in the three separate embodiments shown in FIGURES 1, 2, and 3. There are no pads

in any of the DiStefano et al. layers (FIGURE 2), and, particularly, none can be seen in the second layer to which layers one and two can be connected by their pads as taught by Applicants' device. Please note that FIGURE 2 of DiStefano et al. never mentions pad connections in their specification. *The elements 56a and 58a that the Office claims are pads are flowable conductive reservoir materials that span the interconnect locations (see column 19, lines 29 through 46.*

Also please note that the middle layer 14 (power core layer of Applicants' invention) has vias 16, which are completely filled in FIGURES 1 and 2, but only partially filled in FIGURE 3. By contrast, all of the vias of the second layer of DiStefano et al. are completely filled with flowable materials 56a and 58a.

It should also be observed that claims 4 and 14 describe pads whose surfaces are undercut as shown in embodiment 30. There is no such teaching in DiStefano et al. because they have no pads that can be undercut.

With all due respect to the Office, the laminate structure of DiStefano et al. is entirely different than Applicants' structure as described and claimed. Applicants' vias are connected differently, and the structure with respect to power and signal cores is completely different. DiStefano et al. are particularly silent as to the pad connections both in specification description, and in the drawings, giving pause to the reader that such connections are being read into the specification by the Office. The use of the "pad" descriptors labeled by the Office for 56a and 58a are not plausible, particularly because the term "PAD" is never used in the DiStefano et al. specification.

The rejection based on 35 U.S.C. §102 is respectfully traversed.

It is respectfully requested that claims 1, 2, 4 through 7, 11, 12, and 14 be allowed, and that this application be passed to issue.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

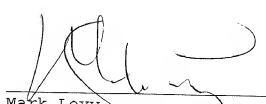
On

3/3/03
(Date of Deposit)

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